*'NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention uses and is suitable for what forms MOSFET of high pressure-proofing and low pressure-proofing at the same substrate about the semiconductor device which integrates and arranges two or more elements, and its manufacture method on the same substrate.
[0002]
[Description of the Prior Art] Conventionally, loading together two or more elements from which pressure-proofing differs on the same semiconductor substrate has been realized for advanced features of semiconductor integrated circuit equipment. An example of such a semiconductor device is shown in drawing 16 .
[0003] Drawing 16 forms pressure-proof low low proof-pressure MOSFET22a in a low proof-pressure field on the semiconductor substrate 1, and forms high proof-pressure MOSFET22b with pressure-proofing higher than the low proof pressure MOSFET in the high proof-pressure field 21.
[0004] Although the low proof pressure MOSFET is formed from a viewpoint of accumulation density and an element property of the minimum processing size in this semiconductor integrated circuit equipment manufacture process, in order to secure high pressure-proofing in the high proof pressure MOSFET, the gate length etc. is formed with a bigger processing size than the low proof pressure MOSFET, and is set up also about the thickness of gate oxide-film 5c more thickly than gate oxide-film 5a of the low proof pressure MOSFET.
[0005] In the former, in order to suppress the leakage current which flows between isolation as high integration progresses, the well field 30 has been high-concentration-ized. However, if the well field 30 is high-concentration-ized, the problem that the pressure-proofing during separation falls conversely will occur, and it will become difficult that separation width of face is compatible with isolation detailed in a field 1 micrometer or less in high separation pressure-proofing.
[0006] Then, as shown in drawing 17 , the well field 3 as the so-called retrospective grade well where the high impurity concentration directly under an isolation layer becomes the highest was formed, the leakage current between isolation was intercepted by making it a high concentration field directly under isolation, and it realized securing diode pressure-proofing by making the bottom of the source drains 15a and 15b into low concentration.
[0007]
[Problem(s) to be Solved by the Invention] However, since it is high concentration only directly under the isolation layer 2 and is low concentration between the other fields 15a and 15b, for example, source drains, when a retrospective grade well is used The problem of it becoming impossible to suppress the elongation of the depletion layer in a low-concentration field, but to suppress the fall (the so-called short channel effect) of the threshold by the punch through between the source drains 15a and 15b in the low proof pressure MOSFET designed with the minimum processing size newly occurs.
[0008] this invention aims at suppressing the short channel effect of MOSFET which deteriorates by using a retrospective grade well in view of the point describing above.
[0009]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, in invention according to claim 1 a low proof-pressure element -- the [the 2nd source field and] -- it consisting of different conductivity types from 2 drain field, and, while having the 2nd retrospective grade well (3 4) by which until formation was carried out more deeply than an isolation insulator layer It is deeper than the 2nd channel field, is shallower than the 2nd retrospective grade well, and is characterized by having the punch-through stop layer (10) which consisted of same conductivity types as the 2nd retrospective grade well.
[0010] Thus, the short channel effect in the low proof-pressure element by using a retrospective grade well can be suppressed by having a punch-through stop layer between a retrospective grade well and a channel field.
[0011] Here, when it is going to load together two or more sorts of MOSFETs from which pressure-proofing differs at the easy process on the same substrate, pressure-proofing of the high proof pressure MOSFET is reduced by existence of the punch-through stop layer inserted with short channel effect suppression of the low proof pressure MOSFET.
[0012] Then, in invention according to claim 2, it is characterized by equipping the low proof-pressure field with the n channel MOS transistor (22a) and the p channel MOS transistor (23a) as a low proof-pressure element, and equipping only the n channel MOS transistor in a low proof-pressure field with the punch-through stop layer among a high proof-pressure field and a low proof-pressure field.

[0013] Thus, the proof-pressure fall of the high proof pressure MOSFET can be prevented by preparing a punch-through stop layer only in a low proof-pressure field.
[0014] In addition, in case the part and semiconductor device which can be communalized will be formed if it is made for the 1st retrospective grade well in a high proof-pressure field and the 2nd retrospective grade well in a low proof-pressure field to have the portion which consists of common wells as shown in a claim 3, abbreviation-ization between manufacturing processes can be attained.
[0015] Moreover, if an isolation insulator layer is formed by embedding an insulator layer in the trench dug in the semiconductor substrate as shown in a claim 4, it can do with the structure which was more suitable for detailed-ization.
[0016] In addition, a claim 5 and invention according to claim 6 are invention of a method which manufactures a claim 1 or the semiconductor device in 4.
[0017] In addition, the sign in the parenthesis of each above-mentioned means shows a correspondence relation with the concrete means of a publication to the operation gestalt mentioned later.
[0018]
[Embodiments of the Invention] (The 1st operation gestalt) The important section cross section of the semiconductor integrated circuit which applied 1 operation gestalt of this invention to drawing 1 is shown. Here, the case where CMOS is formed as a semiconductor integrated circuit is shown.
[0019] The semiconductor substrate 1 consists for example, of a p-type-silicon single crystal, nMOS22a and pMOS23a are formed in the low proof-pressure field 20 as a low proof-pressure element, and nMOS22b and pMOS23b are formed in the high proof-pressure field 21 as a high proof-pressure element. Isolation of each of these low proof-pressure element and a high proof-pressure element is carried out with the STI film (Shallow TrenchIsolation) 2 embedded in the shallow trench 2 formed in the semiconductor substrate 1. The depth of this STI film 2 is set to 0.1-1.0 micrometers. Thus, detailed-ization between isolation can be attained by the isolation by the STI film 2.
[0020] Furthermore, the well field 3 which consists of a p type impurity is formed in the low proof-pressure field 20 and the high proof-pressure field 21 as the same retrospective grade well at nMOS(s) 22a and 22b, and the well field 4 which consists of an n type impurity as the same retrospective grade well is formed in the low proof-pressure field 20 and the high proof-pressure field 21 at pMOS(s) 23a and 23b. These retrospective grade wells 3 and 4 are formed in the position deeper than the STI film 2.
[0021] nMOS(s) 22a and 22b consist of reversed type transistors. Gate insulator layer 5a for low pressure-proofing by which these were formed in the front face of the semiconductor substrate 1, respectively, and gate insulator layer 5c for high pressure-proofing, The gate electrode 6 formed on the gate insulator layers 5a and 5c, and the channel fields 11 and 12 which consist of a p type impurity layer formed in the surface section of the semiconductor substrate 1 under the gate electrode 6, The electric-field relief layer 13 which consists of an n type impurity arranged at the both sides of the channel fields 11 and 12, Source field 15a and drain field 15b which consist of an n type impurity arranged at the both sides of the channel fields 11 and 12, and the side attachment walls 7 and 8 which consist of an insulator arranged at the side of the gate electrode 6 are resembled, and, therefore, it is constituted.
[0022] On the other hand, pMOS(s) 23a and 23b consist of accumulated type transistors. Gate insulator layer 5a for low pressure-proofing and gate insulator layer 5c for high pressure-proofing by which these were formed in the front face of the semiconductor substrate 1, respectively, The gate electrode 6 formed on the gate insulator layers 5a and 5c, and the channel field 11 which consists of a p type impurity layer formed in the surface section of the semiconductor substrate 1 under the gate electrode 6, The electric-field relief layer 14 which consists of a p type impurity formed in the both sides of the channel layer 11, Source field 16a and drain field 16b which consist of a p type impurity arranged at the both sides of the channel layer 11, and the side attachment walls 7 and 8 which consist of an insulator formed in the side of the gate electrode 6 are resembled, and, therefore, it is constituted.
[0023] And it is still shallower than the well field 3 only to nMOS22a of the low proof-pressure field 20, and is deeper than the channel field 12 to it, that is, the punch-through stop layer 10 which consists of a p type impurity [high concentration / field / channel / 12] / in the position which intercepts the elongation of the depletion layer from drain field 15b is constituted.
[0024] Thus, since the constituted semiconductor integrated circuit equips nMOS22a in the low proof-pressure field 20 with the punch-through stop layer [high concentration / field / channel] / 10, the elongation of a depletion layer is suppressed by this punch-through stop layer 10, and it can suppress the short channel effect in nMOS22a by it. For this reason, even if it forms the well layer 3 as a retrospective grade well, the short channel effect can be prevented.
[0025] Moreover, when it is going to load together two or more sorts of MOSFETs from which pressure-proofing differs on the same substrate, you are going to make it communalize the manufacturing process of the low proof-pressure field 20 of the low proof-pressure field 20 and the high proof-pressure field 21 as much as possible to attain abbreviation-ization between manufacturing processes. For example, it is possible to form a punch-through stop layer also in the high proof-pressure field 21 for short channel effect suppression of MOSFET in the low proof-pressure field 20, when forming the punch-through stop layer 10.
[0026] However, when doing in this way, pressure-proofing of MOSFET in the high proof-pressure field 21 will be reduced by existence of a punch-through stop layer. For this reason, as shown in this operation gestalt, the proof-pressure fall of MOSFET in the high proof-pressure field 21 can be prevented by forming the punch-through stop layer 10 only in MOSFET in the low proof-pressure field 20, and not forming a punch-through stop layer in the high proof-pressure field 21.
[0027] Next, the manufacturing process of the semiconductor integrated circuit shown in drawing 1 is shown in drawing 2 -

drawing 13 , and the manufacture method of a semiconductor integrated circuit is explained to them.
[0028] [Process shown in drawing 2] The isolation layer 2 is first formed on the p type semiconductor substrate 1 by the STI method which is well-known technology. Insulators, such as SiO2, are embedded by CVD in the isolation layer 2.
[0029] [Process shown in drawing 3] An ion implantation is carried out so that the peak of concentration may come for the position about [1x1012 to 2x1013cm -] at two where a dose is deeper than the isolation layer 2 to the whole surface in n type impurity, for example, Lynn, through an oxide film 31, and the well field 4 as a 1st retrospective grade well is formed. Thus, abbreviation-ization between processes can be attained by forming a retrospective grade well simultaneously with the low proof-pressure field 20 and the high proof-pressure field 21.
[0030] [Process shown in drawing 4] Patterning is carried out so that the formation schedule field of the nMOS transistors 22a and 22b may carry out opening of the photoresist 32A by the photolithography method. And the ion implantation of p type impurity, for example, the boron, is carried out so that the peak of concentration may come to the position about [1x1012 to 2x1013cm -] at two where a dose is deeper than the isolation layer 2, and the well field 3 is formed. Thereby, nMOS22a in the low proof-pressure field 20 and nMOS22b in the high proof-pressure field 21 are both formed in the same well field 3. Thus, abbreviation-ization between processes can be attained by forming a retrospective grade well simultaneously with the low proof-pressure field 20 and the high proof-pressure field 21.
[0031] [Process shown in drawing 5] Next, by wet etching, after removing an oxide film 31, oxide-film 5b is formed, the high proof-pressure field 21 is covered by photoresist 32B by the photolithography method, and wet etching removes oxide-film 5b on the low proof-pressure field 20.
[0032] [Process which drawing 6 shows] Thermal oxidation is performed after exfoliating photoresist 32B. Thereby, gate oxide-film 5a for low pressure-proofing is formed. At this time, simultaneously, oxidization progresses through oxide-film 5b, and gate oxide-film 5c thicker than gate oxide-film 5a for low pressure-proofing for high pressure-proofing is formed.
[0033] [Process shown in drawing 7] A dose carries out the ion implantation of p type impurity, for example, the boron, all over a wafer about [1x1012 to 2x1012cm -] by two, and the channel layer 11 is formed near the wafer front face.
[0034] [Process shown in drawing 8] By the photolithography method, after carrying out patterning of the photoresist 32C so that the nMOS22a top of the low proof-pressure field 20 may carry out opening, as an ion implantation for threshold adjustment, a dose pours in boron about [1x1012 to 2x1012cm -] by two, and the nMOS channel layer 12 of low pressure-proofing is formed.
[0035] Then, a dose carries out the ion implantation of p type impurity, for example, the boron, to a position deeper than the channel layer 12 by using photoresist 32C as a mask again about [5x1012 to 1x1013cm -] by two, and the punch-through stop layer 10 is formed.
[0036] [Process shown in drawing 9] After removing photoresist 32C, doped polysilicon is deposited, patterning is carried out by the photolithography method, and the gate electrode 6 is formed.
[0037] [Process shown in drawing 10] The front face of the gate electrode 6 is worn by the oxide film 7 by thermal oxidation, all over a wafer, as an n type impurity, the ion implantation of Lynn is carried out and nMOS22a and the electric-field relief layer 13 for 22b are formed by using the gate electrode 6 and an oxide film 7 as a mask.
[0038] [Process shown in drawing 11] By the photolithography method, patterning is carried out so that a pMOS(s)a [23] and 23b top may carry out opening of the photoresist 32D, and the ion implantation of BF2 is carried out as a p type impurity. p type is compensated for the n type electric-field relief layer 13 currently formed in pMOS(s) 23a and 23b by this, and pMOS23a and the electric-field relief layer 14 for 23b are formed. Furthermore, the ion implantation of n type impurity, for example, Lynn etc., is again carried out as a cure against a punch through by using photoresist 32D as a mask, and n- type layer 17 is formed. In addition, it is not necessary to necessarily form this n- type layer 17.
[0039] [Process shown in drawing 12] After depositing the insulator layer which consisted of SiO2 grades, anisotropic etching is performed and a side attachment wall 8 is formed in the side of the gate electrode 6. Then, after forming the oxide film which is not illustrated, the ion implantation of n type impurity, for example, the arsenic, is carried out to nMOS(s) 22a and 22b rather than the electric-field relief layer 13 by the photolithography method at high concentration, and the ion implantation of p type impurity 2, for example, the BF, is carried out to pMOS(s) 23a and 23b rather than the electric-field relief layer 14 at high concentration. Thereby, source field 15a of nMOS(s) 22a and 22b and drain field 15b are formed, and source field 16a of pMOS(s) 23a and 23b and drain field 16b are formed.
[0040] Then, although not illustrated, the usual LSI manufacturing process is performed, and the semiconductor integrated circuit shown in drawing 1 is completed.
[0041] (The 2nd operation gestalt) The cross-section composition of the semiconductor integrated circuit in this operation gestalt is shown in drawing 13 . In the above-mentioned 1st operation gestalt, although the punch-through stop layer 10 is formed only in nMOS22a in the low proof-pressure field 20, with this operation gestalt, the punch-through stop layers 10a and 10b are formed in both nMOS22a in the low proof-pressure field 20, and pMOS23a.
[0042] Thereby, the effect same also about pMOS23a as the above can be acquired by forming punch-through stop layer 10b also about pMOS23a.
[0043] The manufacturing process of the semiconductor integrated circuit shown in drawing 13 is shown in drawing 14 and drawing 15 , and the manufacture method of a semiconductor integrated circuit is explained to them. In addition, only a different portion from the 1st operation gestalt is explained, and the same portion is explained with reference to the 1st operation gestalt here.
[0044] First, the process shown in drawing 2 shown with the 1st operation gestalt - drawing 7 is given. Then, the process shown

in drawing 14 and drawing 15 is performed.

[0045] [Process shown in drawing 14] By the photolithography method, after carrying out patterning of the photoresist 32C so that the nMOS22a top of the low proof-pressure field 20 may carry out opening, as an ion implantation for threshold adjustment, a dose pours in boron about [1x1012 to 2x1012cm -] by two, and the nMOS channel layer 12 of low pressure-proofing is formed.

[0046] Then, a dose carries out the ion implantation of p type impurity, for example, the boron, to a position deeper than the channel layer 12 by using photoresist 32C as a mask again about [5x1012 to 1x1013cm -] by two, and punch-through stop layer 10a is formed.

[0047] [Process shown in drawing 15] By the photolithography method, after carrying out patterning of the photoresist 32E so that the pMOS23a top of the low proof-pressure field 20 may carry out opening, as an ion implantation for threshold adjustment, a dose pours in boron about [1x1012 to 2x1012cm -] by two, and nMOS channel layer 11a of low pressure-proofing is formed.

[0048] Then, a dose carries out the ion implantation of n type impurity, for example, Lynn, to a position deeper than channel layer 11a by using photoresist 32D as a mask again about [5x1012 to 1x1013cm -] by two, and punch-through stop layer 10b is formed.

[0049] Then, the process shown in drawing 10 shown with the 1st operation gestalt - drawing 13 is given, and the semiconductor integrated circuit shown in drawing 14 is completed.

[0050] (others -- operation gestalt) although the above-mentioned operation gestalt showed the example which constituted nMOS from a reversed type transistor and constituted pMOS from an accumulated type transistor, even if it adopts an accumulated type transistor as nMOS, ** is good, and a reversed type transistor may be used for pMOS

[0051] Moreover, although the above-mentioned operation gestalt explained the case where a semiconductor integrated circuit was formed using a p type semiconductor substrate, you may use an n type semiconductor substrate.

[Translation done.]